

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT I, Naoharu Shinozaki, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan have invented certain new and useful improvements in

SEMICONDUCTOR DEVICE AVOIDING MALFUNCTION CAUSED
BY ILLEGAL INPUT

of which the following is a specification : -

1 TITLE OF THE INVENTION
 SEMICONDUCTOR DEVICE AVOIDING MALFUNCTION
 CAUSED BY ILLEGAL INPUT

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to semiconductor devices, and particularly relates to a semiconductor device which allows an operation mode thereof to be set via an external input.

2. Description of the Related Art

Many types of semiconductor devices are provided with a function to set an operation mode thereof. In such semiconductor devices, parameters for setting an operation mode are typically stored in a particular register (hereinafter referred to as a mode register).

Conventional SDRAMs, for example, allow parameters for defining an operation mode of the SDRAMs to be set externally, such parameters including a CAS latency, a burst length, a burst type, etc. In setting these parameters, a mode setting operation is instructed via a command input to an SDRAM, and the parameters are input via an address input so as to write these parameters in a mode register of the SDRAM.

Figs.1A through 1D are illustrative drawings for explaining a mode-register-set operation with respect to a conventional 16M SDRAM. Fig.1A shows a clock signal supplied to an SDRAM. Figs.1B and 1C show a command input and an address input, respectively. As shown in Figs.1B and 1C, a mode-register-set command MRS is input via the command input, and data is supplied to the address input to store the data in the mode register. After inputting the data, an activation command ACT is fed via the command input to put the newly set mode into effect.

Fig.1D shows relations between the data

1 stored in the mode register and the address input. As
shown in Fig.1D, three bits A0 through A2 of the
address input together define the burst length, and a
bit A3 represents the burst type. Further, three bits
5 A4 through A6 of the address input are used for setting
the CAS latency. Bits A7 through A11 are currently not
in use.

Among the parameters, the CAS latency, for
example, is a parameter for defining how long a start
10 of a data-read operation is delayed in response to an
input of a data-read command. The setting of the CAS
latency is made by using the three bits A4 through A6
of the address input as described above. This means
that eight different types of the setting can be made
15 in principle. Settings currently in use, however,
include only three or four different types, so that bit
patterns of the three bits A4 through A6 include unused
patterns.

Fig.2 is a circuit diagram of a conventional
20 latency decoder. A latency decoder is a circuit
included in a mode register. The latency decoder
receives three relevant bits from latches also included
in the mode register for holding the address-input
bits, and decodes these three bits.

25 A latency decoder 200 of Fig.2 includes
inverters 201 through 203, NAND circuits 204 through
207, and inverters 208 through 211. The inverters 201
through 203 receive data bits MRA4 through MRA6,
respectively, which are the address-input bits A4
30 through A6 held by latches. Each of the NAND circuits
204 through 207 receives a non-inverted bit or an
inverted bit with respect to each of the data bits MRA4
through MRA6. The inverters 208 through 211 receive
outputs of the NAND circuits 204 through 207,
35 respectively, and invert these outputs.

The outputs of the inverters 208 through 211
are denoted as decode signals CL1 through CL4,

1 respectively, which correspond to respective bit
patterns of the address-input bits A4 through A6 shown
alongside in the figure. Namely, the decode signal CL1
of the inverter 208, for example, is a signal which
5 becomes HIGH (selection) when the bits A4 through A6
are "100". In the example of Fig.2, the latency
decoder 200 has four outputs, i.e., the decode signals
CL1 through CL4. When the address-input bits A4
through A6 have different bit patterns from those shown
10 in the figure, all the decode signals CL1 through CL4
become LOW (unselected).

In this manner, all the outputs of the
latency decoder 200 end up being unselected when an
undefined bit pattern is input. This is not a unique
15 outcome only for the latency decoder 200, and the same
applies in other decoders in the mode register such as
a burst-length decoder and a burst-type decoder.

When the CAS latency, the burst length, the
burst type, etc., are set in the mode register, entry
20 of an undefined bit pattern which is currently not in
use results in all the decoder outputs from the mode
register ending up being unselected. When such an
undefined setting is made in a conventional
semiconductor device such as an SDRAM, it is possible
25 that the chip carries out an unexpected operation which
is not cited in a catalog. Such an operation may
damage some data stored in memory cells in the case of
memory chips.

Accordingly, there is a need for a
30 semiconductor device which insures a normal operation
thereof even when an undefined setting is made to a
mode register for setting an operation mode of the
device.

35 SUMMARY OF THE INVENTION

Accordingly, it is a general object of the
present invention to provide a semiconductor device

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1 which satisfies the need described above.

It is another and more specific object of the present invention to provide a semiconductor device which insures a normal operation thereof even when an
5 undefined setting is made to a mode register for setting an operation mode of the device.

In order to achieve the above objects according to the present invention, a semiconductor device which allows an input signal thereto to select
10 one of N operation modes, and operates in the one of the N operation modes, includes a selection circuit for selecting an operation mode from the N operation modes when the input signal indicates the operation mode, and for selecting a predetermined operation mode from the N
15 operation modes when the input signal is an undefined signal indicating none of the N operation modes. The semiconductor device further includes an internal circuit operating in an operation mode selected by the selection circuit.

20 In the semiconductor device described above, when an undefined signal is input, one of the N operation modes is selected to prevent an undefined setting from causing an unexpected operation of the semiconductor device.

25 According to an embodiment of the present invention, the selection circuit includes a first circuit for selecting one of predetermined N-1 operation modes among the N operation modes based on the input signal, while a remaining operation mode is
30 selected when this first circuit does not select any one of the N-1 operation modes. In this configuration, an undefined input leads to a selection of the remaining operation mode, thereby preventing an undefined setting from causing an unexpected operation
35 of the semiconductor device.

According to an embodiment of the present invention, a second circuit for selecting the remaining

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1 operation mode based on an output from the first
operation mode is provided in proximity of or within
the internal circuit. This configuration reduces the
number of signal lines from N lines to N-1 lines with
5 respect to the signal transfer of a selected operation
mode from the first circuit to the internal circuit.

According to an embodiment of the present
invention, the selection circuit includes a circuit for
storing the input signal, and a currently stored input
10 signal in this circuit is not updated when an undefined
input is given, thereby preventing an undefined setting
from causing an unexpected operation of the
semiconductor device.

The same objects are also achieved by an
15 equivalent method of selecting one of a plurality of
operation modes in a semiconductor device.

Other objects and further features of the
present invention will be apparent from the following
detailed description when read in conjunction with the
20 accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs.1A through 1D are illustrative drawings
for explaining a mode-register-set operation with
25 respect to a conventional 16M SDRAM;

Fig.2 is a circuit diagram of a conventional
latency decoder;

Fig.3 is a circuit diagram of a latency
decoder of an SDRAM according to a first embodiment of
30 the present invention;

Fig.4 is an illustrative drawing showing a
layout of signal lines of latency-decode signals inside
a semiconductor chip when the latency decoder of Fig.3
is used;

35 Fig.5 is an illustrative drawing showing a
conventional layout of signal lines of latency-decode
signals inside a semiconductor chip when the latency

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Fig.8 is a circuit diagram of the latch control circuit of Fig.7; and

10 Fig.9 is a block diagram of an SDRAM to which
the mode register according to the second embodiment of
the present invention is applied.

15 In the following, principles of the present
invention will be described with reference to the
accompanying drawings.

Fig.3 is a circuit diagram of a latency decoder of an SDRAM according to a first embodiment of the present invention. The present invention is not limited to use in a latency decoder, but can be applied to other decoders for decoding setting data with regard to a mode register for setting an operation mode of a semiconductor device.

25 A latency decoder 10 of Fig.3 includes
inverters 11 through 13, NAND circuits 14 through 16,
inverters 17 through 19, and a NOR circuit 20. The
inverters 11 through 13 receive data bits MRA4 through
MRA6, respectively, which are the address-input bits A4
30 through A6 held by latches of the mode resistor^e. Each
of the NAND circuits 14 through 16 receives a non-
inverted bit or an inverted bit with respect to each of
the data bits MRA4 through MRA6. The inverters 17
through 19 receive outputs of the NAND circuits 14
35 through 16, respectively, and invert these outputs.

The NOR circuit 20 receives the outputs of the inverters 17 through 19, and outputs a HIGH

1 (selection) signal only when all the outputs of the
inverters 17 through 19 are LOW (unselected). The
output of the NOR circuit 20 constitutes the decode
signal CL1, and the outputs of the inverters 17 through
5 19 are the decode signals CL2 through CL4,
respectively. Conditions which make the decode signals
CL1 through CL4 HIGH (selected) are shown by bit
patterns of the address-input bits A4 through A6
alongside the decode signals CL1 through CL4 in the
10 figure.

Compared to the latency decoder 200 of Fig.2,
the latency decoder 10 of Fig.3 according to the first
embodiment has a different condition in which the
decode signal CL1 is selected, i.e., the decode signal
15 CL1 becomes HIGH when the decode signals CL2 through
CL3 are not selected. Namely, the decode signal CL1 is
selected when the address-input bits A4 through A6 are
"100" as in the latency decoder 200 of Fig.2, and,
also, is selected when an undefined setting is made.

20 Accordingly, the use of a decoder having the
configuration as shown in Fig.3 makes it possible to
avoid malfunction of a semiconductor device even when
an undefined setting is made. This is achieved by
allocating undefined settings to one of the defined
25 outputs.

Fig.4 is an illustrative drawing showing a
layout of signal lines of latency-decode signals inside
a semiconductor chip when the latency decoder 10 of
Fig.3 is used. Fig.5 is an illustrative drawing
30 showing a conventional layout of signal lines of
latency-decode signals inside a semiconductor chip when
the latency decoder 200 of Fig.2 is used.

In the layout shown in Fig.5, long-distance
lines 221 through 224 are provided to transfer the
35 decode signals CL1 through CL4 from the latency decoder
200 of Fig.2 to other units inside a chip 220. On the
other hand, the layout of Fig.4 includes long-distance

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1 lines 31 through 33 to transfer only the decode signals
CL2 through CL4 inside a chip 30 from the latency
decoder 10 of Fig.3. Since the decode signal CL1 is
5 selected only when the decode signals CL2 through CL4
are unselected, there is no need to transfer the decode
signal CL1 to other units via a long-distance line.

In each of the units using the latency-decode
signals, the decode signal CL1 can be created based on
the decode signals CL2 through CL4 sent from the
10 latency decoder 10.

Fig.6 is a circuit diagram of an example of a
circuit which creates the decode signal CL1 by using
the decode signals CL2 through CL4. A NOR circuit 35
of Fig.6 receives the decode signals CL2 through CL4,
15 and outputs a HIGH (selection) signal only when all the
received signals are LOW (unselected). Namely, the
output of the NOR circuit 35 is the same as the decode
signal CL1.

The circuit as shown in Fig.6 can be provided
20 for each unit which uses the latency decode signals,
thereby eliminating a need to transfer the decode
signal CL1 via a long-distance line. Since a long-
distance line occupies a larger space than a simple
circuit such as shown in Fig.6, efficient use of space
25 inside a chip is achieved by eliminating one of the
long-distance lines by providing the circuit of Fig.6
for each unit.

The NOR circuit 35 of Fig.6 can be regarded
as the NOR circuit 20 of Fig.3 which is relocated from
30 inside the mode register to each unit which requires
the decode signals. Namely, when a layout as shown in
Fig.4 is used, the NOR circuit 20 of Fig.3 is removed,
and the NOR circuit 35 of Fig.6 is provided for each
unit as a substitute for the removed NOR circuit 20.

35 Fig.7 is a block diagram showing a mode
register and relating elements in an SDRAM according to
a second embodiment of the present invention. Fig.7

1 shows a command-signal-input node 102, an address-
signal-input node 103, a mode-register controlling unit
110, and a mode register 111. The mode register 111
includes a latch control circuit 40, latches 230, a
5 burst-length decoder 240, the latency decoder 200 of
Fig.2, and a burst-type decoder 250. The configuration
of Fig.7 is the same as that of a conventional mode
register and relating elements, except that the latch
control circuit 40 is newly provided.

10 A command signal (see Fig.1B) input to the
command-signal-input node 102 is supplied to the mode-
register controlling unit 110. An address signal (see
Fig.1C) input to the address-signal-input node 103 is
provided to the mode-register controlling unit 110 and
15 the mode register 111. The mode-register controlling
unit 110 outputs an enable signal rgwz in accordance
with timing of the address signal when the received
command signal instructs to set the mode register. In
a conventional configuration, the enable signal rgwz
20 received by the mode register 111 is directly supplied
to the latches 230, and the latches 230 latch the
address signal.

A In the second embodiment of the present
invention, the enable signal ^{RGWZ}~~rgwz~~ received by the mode
25 register 111 is first supplied to the latch control
circuit 40. The latch control circuit 40 receives the
address signal in addition to the enable signal rgwz,
and determines based on the contents of the address
signal whether to provide the enable signal rgwz to the
30 latches 230. In detail, the latch control circuit 40
does not supply the enable signal rgwz to the latches
230 when the address signal shows a bit pattern of an
undefined setting.

Fig.8 is a circuit diagram of the latch
35 control circuit 40. The latch control circuit 40 of
Fig.8 includes inverters 41 through 43, NAND circuits
44 through 47, inverters 48 through 51, a NOR circuit

1 52, inverters 53 and 54, and a NOR circuit 55. The
inverters 41 through 43 receive the bits A4 through A6
of the address signal, respectively. Each of the NAND
circuits 44 through 47 receives a non-inverted bit or
5 an inverted bit with respect to each of the address-
input bits A4 through A6. The inverters 48 through 51
receive outputs of the NAND circuits 44 through 47,
respectively, and invert these outputs.

The outputs of the inverters 48 through 51
10 are decode signals CLa through CLd. Conditions in
which these decode signals CLa through CLd are selected
to turn into HIGH are shown in Fig.8 as bit patterns of
the address-input bits A4 through A6. As can be seen
from a comparison with the bit patterns of the address-
15 input bits A4 through A6 shown in Fig.2, the bit
patterns for the decode signals CLa through CLd of
Fig.8 correspond to undefined bit patterns. Namely,
the inverters 48 through 51 of Fig.8 produce outputs,
one of which is HIGH when an undefined bit pattern is
20 entered.

The NOR circuit 52 receives decode signals
CLa through CLd. The NOR circuit 52 outputs a LOW
signal when one of the decode signals CLa through CLd
is HIGH, and outputs a HIGH signal when all the decode
25 signals CLa through CLd are LOW. The inverter 53
inverts the output of the NOR circuit 52. An output of
the inverter 53 is shown as a control signal stopz.
The control signal stopz becomes HIGH when one of the
decode signals CLa through CLd is HIGH, i.e., when an
30 undefined input is made.

The control signal stopz is supplied to one
input of the two-input NOR circuit 55. The other input
of the NOR circuit 55 receives the inverse of the
enable signal rgwz obtained by the inverter 54.

35 When the control signal stopz is HIGH, the
output of the NOR circuit 55 is LOW at all the times.
The enable signal rgwz is thus blocked by the NOR

1 circuit 55. When the control signal stopz is LOW, the
NOR circuit 55 serves as an inverter for the inverse of
the enable signal rgwz. The NOR circuit 55 thus
5 outputs the enable signal rgwz by inverting the inverse
of the enable signal rgwz.

The output of the NOR circuit 55 is supplied
to the latches 230 as a latch-control signal rgwsz (see
Fig.7). In this manner, the latch control circuit 40
blocks the enable signal rgwz when an undefined input
10 is made, and outputs the enable signal rgwz as the
latch-control signal rgwsz when a defined input is
made. Having received the latch-control signal rgwsz,
the latches 230 latch the address-input bits A0 through
A06.

15 As described above, the mode register 111
according to the second embodiment of the present
invention shown in Fig.7 and Fig.8 can avoid
malfunction of an SDRAM when an undefined input is
attempted because no setting is made to the CAS latency
20 when an undefined input is made.

In the configuration shown in Fig.7 and
Fig.8, when an undefined input is made with respect to
a burst length, the undefined input is held by the
latches 230, and is decoded by the burst-length decoder
25 240 to be output. (There is no undefined setting for a
burst type since the burst type is represented by only
one bit.) If one wishes to provide an anti-malfunction
mechanism also for the burst length, therefore, one may
modify the circuit of Fig.8 so as to detect an
30 undefined input with respect to the bits A0 through A2.

The second embodiment of the present
invention has a configuration such that when an
undefined input is made, data writing to the mode
register is prohibited by detecting the undefined
35 input. It is apparent that this configuration is not
limited to application only to a mode register of
SDRAMs, but can be applied to various semiconductor

1 devices.

Fig.9 is a block diagram of an SDRAM to which the mode register according to the second embodiment of the present invention is applied. The SDRAM of Fig.9 includes a clock-signal-input node 101, the command-signal-input node 102, the address-signal-input node 103, a data-signal-input/output node 104, an internal-clock-generation unit 105, a command-input buffer 106, an address-input buffer 107, a data-output buffer 108, a data-input buffer 109, the mode-register controlling unit 110, the mode register 111 shown in Fig.7, a command decoding unit 112, an address decoding unit 113, pipelines 114 and 115, a write-control unit 116, a write amplifier 117, a sense amplifier 118, a read/write-control unit 119, a read amplifier 120, and a memory-cell array 121.

The SDRAM of Fig.9 has the same configuration as that of a conventional SDRAM, except that the mode register 111 of the present invention is used.

In the following, operations of the SDRAM of Fig.9 will be described in brief. A clock signal input to the clock-signal-input node 101 is supplied to the internal-clock-generation unit 105, which generates various internal clock signals for controlling the internal circuits. Based on internal clock signals generated by the internal-clock-generation unit 105, the command-input buffer 106, the address-input buffer 107, and the data-input buffer 109 read a command signal, an address signal, and a data signal from the command-signal-input node 102, the address-signal-input node 103, and the data-signal-input/output node 104, respectively.

The command signal is supplied from the command-input buffer 106 to the command decoding unit 112 to be decoded. Based on the decoding results, the internal circuits are controlled. When a mode-register setting command is provided as a command, the mode-

1 register controlling unit 110 writes an address signal
from the address-input buffer 107 in the mode register
111 in response to the mode-register setting command.

5 The address signal is supplied from the
address-input buffer 107 to the address decoding unit
113 for decoding. Based on the address decoding
results, the memory-cell array 121 is accessed at an
indicated address thereof.

10 The data signal is stored in the memory-cell
array 121 at the indicated address thereof, supplied
from the data-input buffer 109 via the write amplifier
117 and the sense amplifier 118. On the other hand,
data read from the memory-cell array 121 at the
15 indicated address thereof is supplied to the data-
output buffer 108 via the sense amplifier 118, the read
amplifier 120, and the pipelines 114 and 115. The
data-output buffer 108 outputs the data to the data-
signal-input/output node 104 based on an internal clock
generated by the internal-clock-generation unit 105.

20 The write-control unit 116 supplies a control
signal to the read/write-control unit 119 in accordance
with the command decoding results of the command
decoding unit 112. Also, based on the command decoding
results, the write-control unit 116 controls the data-
25 input buffer 109.

The read/write-control unit 119 generates
control signals such as a write signal Write, a read
signal Read, a column-line selecting signal (not
shown), etc. The column-line selecting signal, for
30 example, is supplied to the sense amplifier 118 which
is comprised of a plurality of sense amplifiers, and
allows data to be written in or read from selected
sense amplifiers for a predetermined time period. The
write signal Write is supplied to the write amplifier
35 117 so as to provide the input data from the data-input
buffer 109 to global data bus GDB0 and GDB1 at a
predetermined timing. The read signal Read is supplied

1 to the read amplifier 120 so as to provide the read
data from the global data bus GDB0 and GDB1 to the
pipeline 115 at a predetermined timing.

5 The mode register 111 stores settings of the
burst length, the burst type, the CAS latency, etc., as
previously described. As for the CAS latency, for
example, the mode register 111 outputs the CAS-latency
indicating signals (decode signals) CL1 through CL4 for
10 indicating which CAS latency is being used. (When the
number of CAS latencies which can be set is more than
4, a CAS-latency indicating signal CL5 and so on are
also generated.) Based on the CAS-latency indicating
signals CL1 through CL4, the read/write-control unit
119 controls the timing of a data-read operation.

15 As described in connection with Fig.7 and
Fig.8, when an attempt is made to set an undefined CAS
latency in the mode register 111, this undefined CAS
latency is prevented from being written in the mode
register 111. In the SDRAM of Fig.9, therefore, a
20 malfunction can be avoided even when an undefined input
is attempted for the CAS latency. Further, it is
obvious that the function of preventing undefined input
can be provided for other parameters such as a
parameter for the burst length in addition to the CAS
25 latency.

In the SDRAM of Fig.9, the mode register 111
of Fig.7 may be replaced by a conventional mode
register, and the latency decoder of Fig.3 may be
provided in this replacing mode register. In this
30 case, when an undefined setting is attempted for the
CAS latency, the CAS-latency indicating signal CL1, for
example, is selected, thereby avoiding a malfunction of
the SDRAM. In this configuration, signal lines inside
the SDRAM for transferring the CAS-latency indicating
35 signals may be provided only for the CAS-latency
indicating signals CL2 through CL4, and the NOR circuit
35 of Fig.6 may be provided in relevant circuit units

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1 such as the read/write-control unit 119.

Further, the present invention is not limited
to these embodiments, but variations and modifications
may be made without departing from the scope of the
5 present invention.

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